



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, CA 90638
 Phone: (562) 404-4474 * Fax: (562) 404-1773
 ssdi@ssdi-power.com * www.ssdi-power.com

SFS07050 thru SFS07400 Series

**7 AMP SILICON CONTROLLED RECTIFIER
 50 – 400 VOLTS**

| Designer's Data Sheet | |
|--|-------------------------|
| Part Number/Ordering Information ^{1/} | |
| SFS07 | |
| | Screening ^{2/} |
| | Package |
| | Voltage/Family |
| | |

___ = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level
 ___ = TO-5
 S.5 = SMD.5
 G = Cerpack

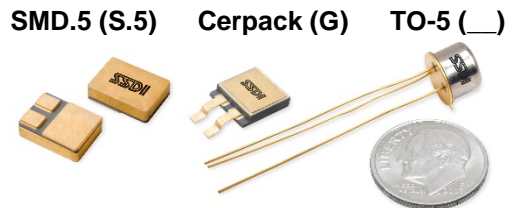
050 = 50 V 250 = 250 V
 100 = 100 V 300 = 300 V
 200 = 200 V 400 = 400 V

- FEATURES:**
- Low-Level Gate Characteristics
 - $I_{GT} = 20 \mu A$ (typical) @ 25°C
 - Low Holding Current $I_H = 1.25 \text{ mA}$ (typ) @ 25°C
 - Anode Common to Case
 - Hermetically Sealed

| MAXIMUM RATINGS | | Symbol | Value | Unit |
|---|----------------|------------------------|-------------|------|
| Peak Repetitive Reverse Voltage and DC Blocking Voltage | SFS07050 | V_{DRM} V_{RRM} | 50 | V |
| | SFS07100 | | 100 | |
| | SFS07200 | | 200 | |
| | SFS07250 | | 250 | |
| | SFS07300 | | 300 | |
| | SFS07400 | | 400 | |
| Non-Repetitive Peak Reverse Blocking Voltage $t < 5.0 \text{ ms}$ | SFS07050 | V_{RSM} | 75 | V |
| | SFS07100 | | 150 | |
| | SFS07200 | | 300 | |
| | SFS07250 | | 350 | |
| | SFS07300 | | 400 | |
| | SFS07400 | | 500 | |
| RMS On-State Current All Conduction Angles | | $I_{T(RMS)}$ | 7 | A |
| Peak Non-Repetitive Surge Current One Cycle, 60 Hz, $T_c = 80^\circ C$ | | I_{TSM} | 80 | A |
| Peak Gate Power | | P_{GM} | 20 | W |
| Average Gate Power | | $P_{G(AV)}$ | 0.5 | W |
| Peak Gate Current | | I_{GM} | 1 | A |
| Peak Gate Voltage | | V_{GM} | 6.0 | V |
| Operating Junction Temperature Range | | T_J | -55 to +125 | °C |
| Storage Temperature Range | | T_{stg} | -55 to +150 | °C |
| Thermal Resistance, Junction to Case | TO-5 | $R_{\theta JC}$ | 10 (6 typ) | °C/W |
| | SMD.5, Cerpack | | 3.5 (2 typ) | |

NOTES:

- 1/ For ordering information, price, operating curves, and availability - Contact factory.
- 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
- 3/ Unless otherwise specified, all electrical characteristics @ 25°C.





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| ELECTRICAL CHARACTERISTICS | | Symbol | Min | Typical | Max | Unit |
|---|---------------------------------------|-----------|-----|---------|-----|--------------|
| Peak Reverse Blocking Current | Rated V_{RRM} , $T_C = 25^\circ C$ | I_{RRM} | — | 0.2 | 1 | μA |
| | Rated V_{RRM} , $T_C = 110^\circ C$ | | | 25 | 500 | |
| Peak Forward Blocking Current | Rated V_{RRM} , $T_C = 25^\circ C$ | I_{DRM} | — | 0.2 | 1 | μA |
| | Rated V_{RRM} , $T_C = 110^\circ C$ | | | 40 | 750 | |
| Peak On-State Voltage $I_F = 7 A$, $T_C = 25^\circ C$ | | V_{TM} | — | 2.1 | 2.2 | V |
| Gate Trigger Current $V_D = 6 V_{DC}$, $R_L = 100 \Omega$, $T_C = 25^\circ C$ | | I_{GT} | — | 20 | 200 | μA |
| Gate Trigger Voltage $V_D = 6 V_{DC}$, $R_L = 100 \Omega$, $T_C = 25^\circ C$ | | V_{GT} | — | 0.51 | 0.8 | V |
| Gate Controlled Turn-on Time $I_G = 10 mA$, $T_C = 25^\circ C$ | | t_{GT} | — | 0.6 | 1.2 | μsec |
| Critical Rate of Rise of Off-State Voltage Open gate, $V = 100 V$, $T_C = 100^\circ C$ | | dV/dt | 100 | 270 | — | V/ μsec |
| Holding Current $V_D = 6 V_{DC}$, $T_C = 25^\circ C$ | | I_{HO} | — | 1.25 | 10 | mA |

NOTES: * RGK current is not included in measurement

| <p>Case Outline: TO-5</p> | <p>Case Outline: SMD.5</p> | | | | | | | | | | | | | | | | |
|-------------------------------------|---|---------|---------------------|--------|--------|------|---------|------|-------|-------|-------|---------|------|---------|-------|---------|------|
| <p>Case Outline: Cerpack</p> | <table border="1"> <thead> <tr> <th>PACKAGE</th> <th>PIN 1 / Bottom Pad:</th> <th>PIN 2:</th> <th>PIN 3:</th> </tr> </thead> <tbody> <tr> <td>TO-5</td> <td>CATHODE</td> <td>GATE</td> <td>ANODE</td> </tr> <tr> <td>SMD.5</td> <td>ANODE</td> <td>CATHODE</td> <td>GATE</td> </tr> <tr> <td>Cerpack</td> <td>ANODE</td> <td>CATHODE</td> <td>GATE</td> </tr> </tbody> </table> <p>*For information on curves, contact the Factory Representative for Engineering Assistance.</p> | PACKAGE | PIN 1 / Bottom Pad: | PIN 2: | PIN 3: | TO-5 | CATHODE | GATE | ANODE | SMD.5 | ANODE | CATHODE | GATE | Cerpack | ANODE | CATHODE | GATE |
| PACKAGE | PIN 1 / Bottom Pad: | PIN 2: | PIN 3: | | | | | | | | | | | | | | |
| TO-5 | CATHODE | GATE | ANODE | | | | | | | | | | | | | | |
| SMD.5 | ANODE | CATHODE | GATE | | | | | | | | | | | | | | |
| Cerpack | ANODE | CATHODE | GATE | | | | | | | | | | | | | | |

NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: SCR011D

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