Solid State Devices, Inc.
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SPH35A36-20

3.5 AMP
Adjustable Output Synchronous
Step Down DC-DC Converter

Designer's Data Sheet

Part Number / Ordering Information 1/

SPH35A36-20

Screening 2/
__ = Not Screened
H = Hirel

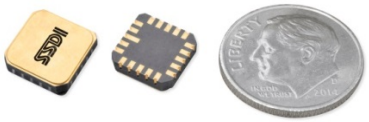
Package : -20 = LCC20

Features:
- ±1% Output voltage tolerance, T_J = 25°C
- Input voltage range of 3.9 V to 36 V, transient up to 42 V
- Low EMI and switch noise
- External frequency synchronization
- Built-in compensation, soft start, current limit, thermal shutdown and UVLO
- Isolated hermetically sealed ceramic power package

MAXIMUM RATINGS 4/ 5/	Symbol	Min	Max	Units
AVI 3/, **PVI** 3/		-0.3	40	V
SYN 3/ 8/, **EBL** 3/ 8/		-0.3	40	V
PWM 8/ **to AGND/GND**		-0.3	40	V
BIA,FBK to AGND/GND		-0.3	16	V
BOOT to OUT **VC to AGND/GND**		-0.3	3.6	V
$\overline{\text{RST}}$ to AGND/GND		-0.3	8	V
SW to AGND/GND		-0.3	Vin + 0.3	V
$\overline{\text{RST}}$ sink current		-	10	mA
Junction Temperature **Storage Temperature**	T_J T_{STG}	-55 -55	150 125	°C
Thermal Resistance **Junction to case (lid)** **Junction to case (edge)**	$R_{\theta JC(lid)}$ $R_{\theta JC(edge)}$	-	3.5 4	°C/W

Notes:
1/ For ordering information, price, operating curves, and availability, contact factory.
2/ High reliability screening – contract factory for screening flow.
3/ Referenced to AGND & GND; can sustain max 42V for ≤ 500 ms, d.c.≤ 0.01%
4/ Unless otherwise specified, limits apply to full junction temperature range.
5/ Limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_j = 25°C and are provided for reference only. Unless otherwise specified, V_{IN} = 13.5 V. Unless otherwise specified, parameters are not ensured in production testing.
6/ Ensured in production testing at T_A = 25°C.
7/ For additional technical information and assistance, contact factory.
8/ Do not allow to exceed AVI or PVI by more than 0.3 V.
9/ Minimum 3.5 V is possible, see System Characteristics table.
10/ Output voltage must not be allowed to fall below 0 V during normal operation.
11/ Ensured by design provided that the component values in the typical application circuit are used.

LCC20 (-20)



RECOMMENDED OPERATING CONDITIONS 4/ 5/	Symbol	Min	Typ	Max	Unit
Input Voltage after start-up 6/ 9/	V_{IN}	3.9	-	36	V
Output Voltage 6/ 10/	V_{OUT}	3.3	-	15	V
Load Current	I_L	-	-	3.5	A
Junction Temperature 1000hrs lifetime 408hrs lifetime	T_J	-55 -55	- -	125 150	°C

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ELECTRICAL CHARACTERISTICS [4/] [5/]		Symbol	Min	Typ	Max	Unit
Initial output voltage accuracy	V_{IN} = 3.8 V to 36 V, T_J = 25°C V_{IN} = 3.8 V to 36 V	V_{FBK1} V_{FBK2}	-1 -1.5	- -	1 1.5	%
Operating quiescent current	V_{IN} = 13.5 V, V_{BIA} = 5 V	I_Q	-	6	-	µA
Bias current	V_{IN} = 13.5 V, V_{BIA} = 3.3 V or 5 V, PWM = 0	I_B	-	35	-	µA
Shutdown quiescent current	at V_{IN}, EBL ≤ 0.4 V, T_J = 25°C	I_{SD}	-	2	-	µA
Vin-Operate, minimum input voltage to operate	Rising Falling Hysteresis	$V_{IN-OPER-R}$ $V_{IN-OPER-F}$ $V_{IN-OPER-H}$	3.2 2.95 0.28	3.55 3.25 0.3	3.95 3.55 0.4	V
$\overline{\text{RST}}$ threshold voltage	rising,% of Vout, upper threshold falling,% of Vout, lower threshold $\overline{\text{RST}}$ lower threshold from steady state	V_{RST-U} V_{RST-L} V_{RST-M}	105 92 -	107 94 -	110 96.5 96	%
$\overline{\text{RST}}$ hysteresis	Percent of V_{OUT} setpoint	V_{RST-M}	-	±1	-	
Minimum input voltage for proper $\overline{\text{RST}}$ function	50 µA pullup to $\overline{\text{RST}}$, EBL = 0 V, T_J = 25°C	$V_{RST-valid}$	-	-	1.5	V
Low level $\overline{\text{RST}}$ function output voltage	50 µA pullup to $\overline{\text{RST}}$ pin, V_{IN} = 1.5 V, EN = 0 V 0.5 mA pullup to $\overline{\text{RST}}$ pin, V_{IN} = 13.5 V, EN = 0 V 1 mA pullup to $\overline{\text{RST}}$ pin, V_{IN} = 13.5 V, EN = 3.3 V	V_{OL1} V_{OL2} V_{OL3}	- - -	- - -	0.4 0.4 0.4	V
PWM input threshold voltage	PWM input high (MODE = PWM) PWM input low (MODE = AUTO diode emulation) PWM input hysteresis	V_{PWM1} V_{PWM2} V_{PWM3}	1.5 - 0.15	- - -	- 0.4 1	V
Switching frequency	VIN = 13.5 V, center frequency PWM operation	F_{OUT}	1.85	2.1	2.35	MHz
Sync frequency range		F_{SYN}	1.9	2.1	2.3	MHz
Sync input duty cycle range	High state input < 5.5 V and > 2.3 V	D_{SYN}	25	-	75	%
PWM leakage current	V_{IN} = 13.5 V, V_{PWM} = 3.3 V V_{IN} = V_{PWM} = 13.5 V	I_{PWM1} I_{PWM2}	- -	1 5	- -	µA
SYNC leakage current	V_{IN} = 13.5 V, V_{SYN} = 3.3 V V_{IN} = V_{SYN} = 13.5 V	I_{SYN1} I_{SYN2}	- -	1 5	- -	µA
Output current limit	High-side Low-side	I_{L-HS} I_{L-LS}	4.5 3.5	6 4.5	7.5 5.1	A
Zero-cross current limit PWM = low		I_{L-ZC}	-	-0.02	-	A
Negative current limit PWM = high		I_{L-NEG}	-	-1.5	-	A

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ELECTRICAL CHARACTERISTICS [4/] [5/]		Symbol	Min	Typ	Max	Unit
Power output on-resistance	V_{IN} = 13 V, I_L = 1 A	$R_{DSon-HS}$ $R_{DSon-LS}$	- -	60 40	130 80	mΩ
Enable input threshold voltage - rising		V_{EBL}	1.7	-	2	V
Enable threshold hysteresis		V_{EBL_HYST}	0.45	-	0.55	V
Enable wake-up threshold		V_{EBL_WAKE}	0.4	-	-	V
EBL pin input current	V_{IN} = V_{EBL} = 13.5 V	I_{EBL}	-	2	5	µA
Internal VC voltage	V_{IN} 13.5 V, V_{BIA} = 0 V V_{IN} = 13.5 V, V_{BIA} = 3.3 V	V_{C1} V_{C2}	- -	3.05 3.15	- -	V
Internal VC input under-voltage lockout	V_{IN} rising Hysteresis below V_{C-UVLO}	V_{C_UVLO1} V_{C_UVLO2}	- -	2.7 185	- -	V mV
Input current from FBK to AGND	FBK = 1 V	I_{FBK}	-	20	-	nA
Reference voltage to FBK	T_J = 25°C	V_{REF}	0.993	1	1.007	V
RDson of $\overline{\text{RST}}$ output	FBK = low, $\overline{\text{RST}}$ pin = 1 mA	R_{RST}	-	50	85	Ω
Voltage Syn		V_{SYN-IH} V_{SYN-IL} $V_{SYN-HYST}$	1.5 - 0.15	- - -	- 0.4 1	V
Thermal shutdown thresholds	Rising Hysteresis	T_{SD1} T_{SD2}	155 -	- 15	175 -	°C
Maximum output duty cycle	F_{SW} = 2.1 MHz While in dropout	D_{MAX1} D_{MAX2}	- 98	80 -	- -	%

SYSTEM CHARACTERISTICS [4/] [5/] [11/]		Symbol	Min	Typ	Max	Unit
Min. input voltage for full functionality [6/]	1.5 A, V_{OUT} = 3.3 V +2/–3% 3.5 A, V_{OUT} = 3.3 V +2/–3%	$V_{IN-MIN1}$ $V_{IN-MIN2}$	- -	3.5 3.9	- -	V
Output voltage [6/]	V_{IN} = V_{OUT}+1 V to 3 V, I_{OUT} = 3.5 A	V_{OUT}	-2.25	-	2.25	%
Input current to VIN	V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A PWM = 0 V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 0 A PWM = 0	I_{Q-VIN1} I_{Q-VIN2}	- -	15 20	40 -	µA
Min VIN-VOUT to maintain regulation accuracy w/o inductor DCR drop	V_{OUT} = 3.3 V / 5 V, I_{OUT}= 3.5 A, +2/–3% output accuracy	V_{DROP1}	-	0.35	0.6	V
Min VIN-VOUT to maintain F_{SW} ≥ 1.85 MHz w/o inductor DCR drop	V_{OUT} = 3.3 V / 5 V, I_{OUT} = 3.5 A, F_{SW} = 1.85 MHz, 2% regulation accuracy	V_{DROP2}	-	1.1	1.4	V
Typical Efficiency without inductor Loss [6/]	V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 3.5 A V_{IN} = 13.5 V, V_{OUT} = 3.3 V, I_{OUT} = 3.5 A V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 0.1 A	E_{ff1} E_{ff2} E_{ff3}	- - -	90 84 88	- - -	%

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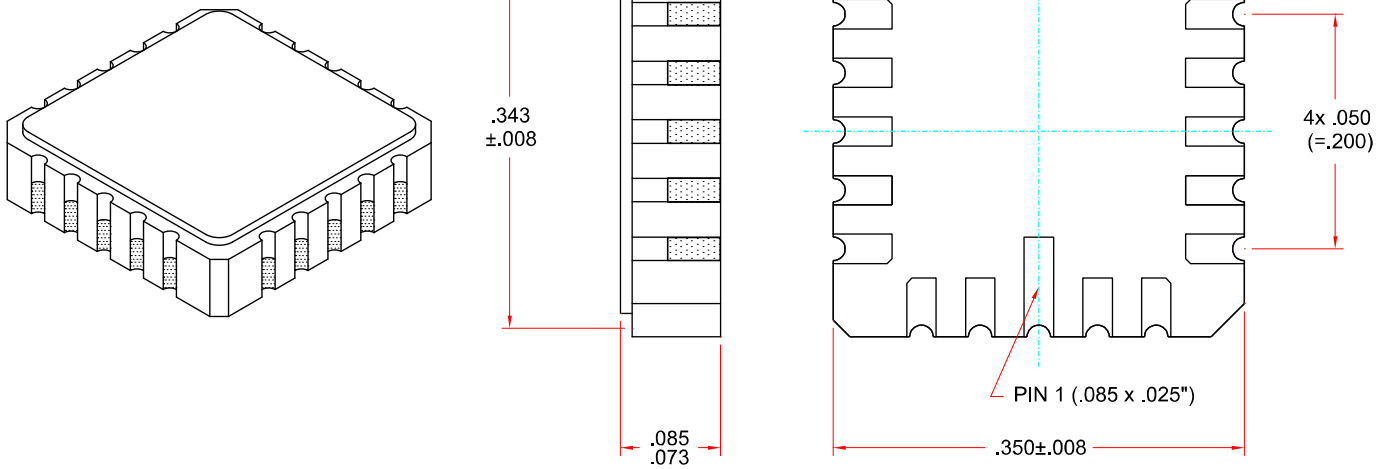
TIMING CHARACTERISTICS [4/ 5/]		Symbol	Min	Typ	Max	Unit
Minimum switch on time	V_{IN} = 18 V, I_L =1 A	t_{ON}	-	65	-	ns
Minimum switch off time	V_{IN} = 3.8 V, I_L =1 A	t_{OFF}	-	60	-	ns
Delay time to $\overline{\text{RST}}$ high signal		$t_{RST\text{-}act}$	2	3	4	ms
Glitch filter time for $\overline{\text{RST}}$ function		$t_{RST\text{-}filter}$	12	25	45	µs
Soft-Start Time from first switching pulse to VREF at 90%		t_{SS}	2	3.2	5	ms
Turn-on delay, C_{VC} = 2.2 µF		t_{EBL}	-	1	-	ms
Short circuit wait time (*hiccup* time)		t_W	-	6	-	ms
Change transition time, 20mA load, V_{IN} = 13.5 V	AUTO to PWM MODE PWM to AUTO MODE	t_{PWM1} t_{PWM2}	- -	100 80	- -	µs

Package Outline:



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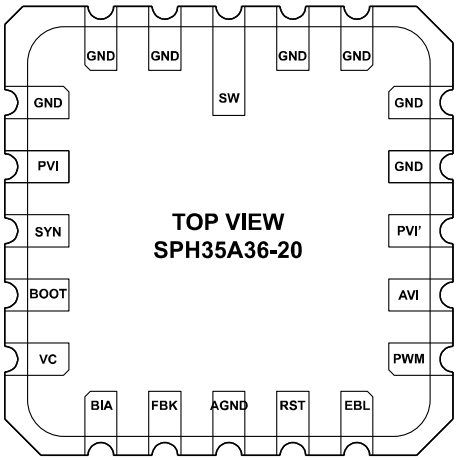
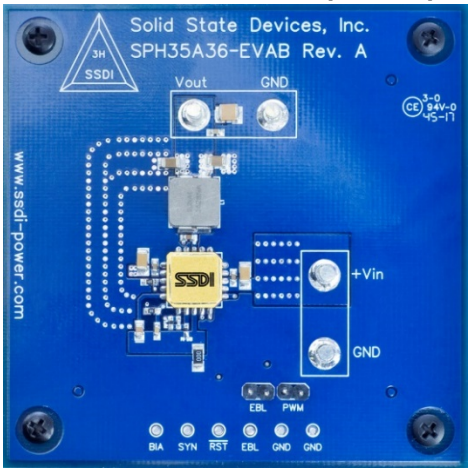
Pin Assignment and Descriptions 7/:

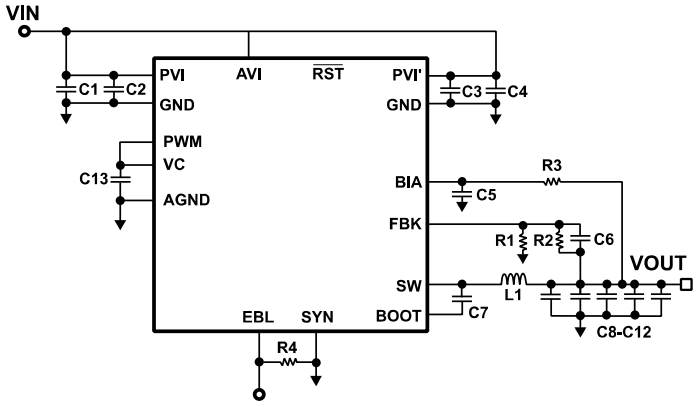


VC	Internal 3.1-V LDO output. Connect a high-quality 4.7-µF capacitor from this pin to AGND.
BOOT	Bootstrap capacitor connection for gate drivers. Connect a high quality 470-nF capacitor from this pin to the SW pin.
SYN	Synchronization input to regulator. Used to synchronize the device switching frequency to a system clock. Triggers on rising edge of external clock; frequency must be in the range of 1.9 MHz and 2.3 MHz. GND if not used
PVI, PVI'	Input supply to regulator. Connect input bypass capacitors directly to this pin and GND pins. Connect PVIN pins directly together at PCB.
GND	Power ground to internal MOSFET. These pins must be tied together on the PCB. Connect GND directly together at PCB. Connect to AGND and system ground.
SW	Regulator switch node. Connect to power inductor.
AVI	Analog input, Connect to PVI on PCB.
PWM	Do not float. Mode control input of regulator. High = PWM, low = Automatic light load mode.
NC	No internal connection
EBL	Enable input to regulator. High = on, Low = off. Can be connected to V_{IN}. Do not float.
$\overline{RST}$	Open drain reset output flag. Connect to suitable voltage supply through a current limiting resistor. High = regulator OK, Low = regulator fault. Goes low when EBL = low.
AGND	Analog ground for regulator and system. All electrical parameters are measured with respect to this pin. Connect to GND on PCB
FBK	Feedback input to regulator. Connect to output voltage node for fixed VOUT options. Connect to feedback voltage divider for adjustable option.
BIA	Input to auxiliary bias regulator. Connect to output voltage node.

Evaluation Board Available Upon Request:



Typical Application Circuit 7/:



Tolerances
C1-C12 = +/-10%; C13= +/-20%; R1 & R2 = +/-1%; R3 & R4 = +/-5%

APPLICATION CIRCUIT

Recommended Values
C1,C4 = 10 uF
C2,C3,C5 = 0.1 uF
C6 = 12 pF
C7 = 0.47 uF
C8-C12 = 22 uF
C13 = 4.7 uF
L1 = 2.2 uH or 4.4 uH (10 V V_{OUT})
R3 = 3 Ω
R4 = EBL pull down resistor
R1,R2 = select values to obtain desired V_{OUT} per

$$\text{Output Voltage} = V_{ref} \times \frac{R1 + R2}{R1}$$

where Vref is FBK node voltage, ~1 V

Basic PCB Layout Guidelines

The PCB lay-out is critical for optimal performance of the circuit.

- Use two parallel input loops to ground for PVI and PVI' to cut parasitic input inductance. Place capacitors C2 & C3 as close to possible to converter.
- Place caps for VC & BIA close to their respective pins. Ensure AGND pin connects first to these caps before connecting to GND.
- Place BOOT capacitor with smallest parasitic loop to reduce common mode noise. Placing a small R_{BOOT} resistor (< 3 Ω is recommended) in series to BOOT will reduce EMI. (Note: this R_{BOOT} resistor option is not incorporated on the test board).
- Place R1 & R2 resistor dividers close to FBK pin and to AGND pin of the device. Use dedicated feedback trace and away from Output node and BOOT capacitor to avoid any cross coupling into sensitive analog feedback.
- Use dedicated BIA trace to avoid noise into feedback trace
- Use a 3-Ω to 5-Ω resistor between the output and BIA if the load is far from the output of the converter or inductive shorts on the output are possible.
- Use well connected large 2-oz. TOP and BOTTOM copper.
- Minimize output node and BOOT area for lowest EMI common mode noise.
- For lowest EMI place input and output wires on same side of PCB, using EMI filter and place away from output node.