



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
Phone: (562) 404-4474 * Fax: (562) 404-1773
ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SPH **32** **70** **FP** **Screening** ^{2/}
Lead Bend Options
 — = Straight
 UB = Up Bend
 DB = Down Bend
Package ^{3/}
 FP = Flat pack – 12 Pin Package
Voltage
 70 = 700 V
Current
 32 = 32 A

SPH3270FP

32 AMP , 700 Volts, 0.09 Ω
Half-Bridge, N-Channel MOSFET
Hi-Rel POWER HYBRID

Features:

- Rugged poly-Si gate
- Lowest ON-resistance in the Industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- Improved ($R_{DS(ON)}$, Q_G) Figure of Merit
- Class H, K Screening Available ^{2/}
- Consult Factory for Special Requirements such as Built-in Zener Diode Protection, Gate Resistor, Anti-Parallel Diode for Faster Switching, etc.

Typical Applications:

- Airborne/Aerospace
- Motor Controls
- Inverters

Maximum Ratings (per side) ^{3/}		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	700	V
Gate – Source Voltage	continuous	V_{GS}	+20	V
	transient		+30	
Continuous Drain Current (Lead $\leq$ 0.3", Top Limited)	@ $T_C = 25^\circ C$	I_{D1}	32	A
	@ $T_C = 100^\circ C$	I_{D2}	20	
Pulsed Drain Current (Pulse Width/Top Limited)	@ $T_C = 25^\circ C$	I_{D3}	100	A
Single and Repetitive Avalanche Energy	@ L = 0.1 mH	E_{AS}	1100	mJ
		E_{AR}	1.5	
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	208	W
Operating & Storage Temperature		$T_{OP} \text{ \& } T_{STG}$	-55 to +150	$^\circ C$
Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.6 (typ 0.3)	$^\circ C/W$

NOTES:

*Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.

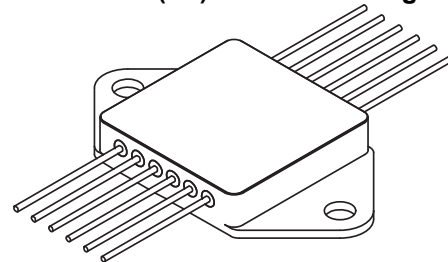
1/ For ordering information, price, and availability – contact factory.

2/ Screening based on MIL-PRF-38534. Screening flows available on request.

3/ Unless otherwise specified, all electrical characteristics @25 $^\circ C$.

4/ All Drain and Source Pins are utilized

Flat Pack (FP) – 12 Pin Package



NOTE: All specifications are subject to change without notification.
 SCD's for these devices should be reviewed by SSDI prior to release.

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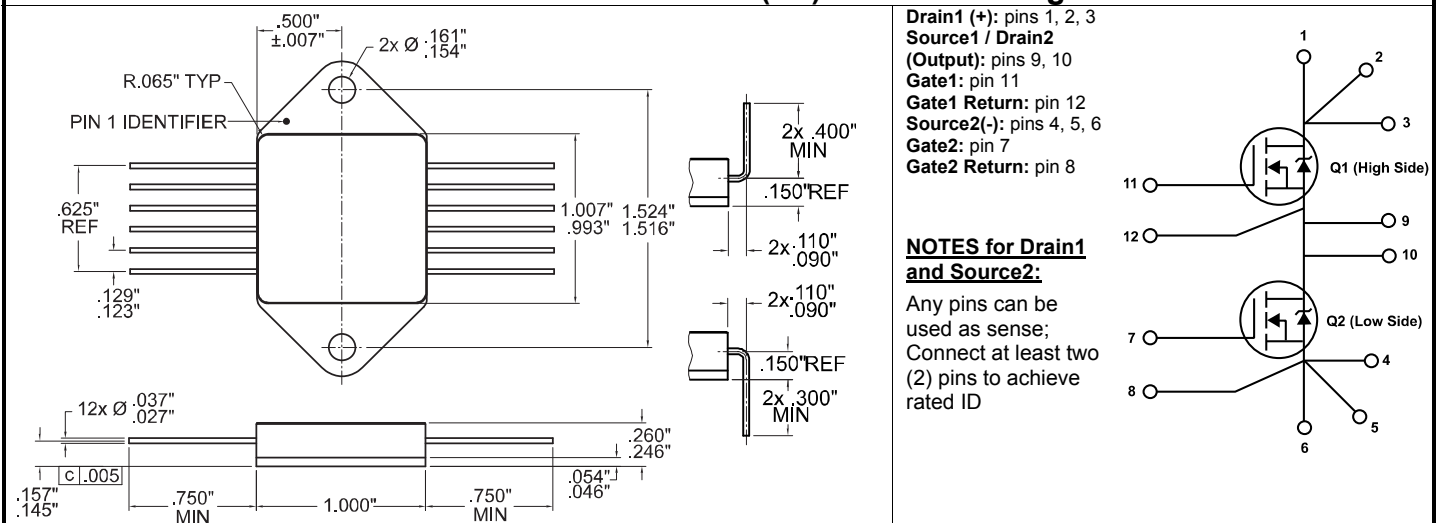
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SPH3270FP

Electrical Characteristics (per side) ^{3/}		Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage	$V_{GS} = 0V, I_D = 1 \text{ mA}$	BV_{DSS}	700	740	—	V
Drain to Source On State Resistance^{4/}	$V_{GS} = 10V, I_D = 18A, T_j = 25^\circ C$	$R_{DS(on)}$	—	88	94	mΩ
	$V_{GS} = 10V, I_D = 18A, T_j = 125^\circ C$		—	168	—	
			—	—	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1.75mA, T_j = 25^\circ C$	$V_{GS(th)}$	3.5	4.2	4.5	V
	$V_{DS} = V_{GS}, I_D = 1.75mA, T_j = 125^\circ C$		2.5	3.4	—	
	$V_{DS} = V_{GS}, I_D = 1.75mA, T_j = -55^\circ C$		—	4.7	5.5	
Gate to Source Leakage	$V_{GS} = \pm 20V, T_j = 25^\circ C$	I_{GSS}	—	10	± 100	nA
	$V_{GS} = \pm 20V, T_j = 125^\circ C$		—	30	—	
Zero Gate Voltage Drain Current	$V_{DS} = 650V, V_{GS} = 0V, T_j = 25^\circ C$	I_{DSS}	—	1	25	μA
	$V_{DS} = 650V, V_{GS} = 0V, T_j = 125^\circ C$		—	15	150	
			—	—	—	
Total Gate Charge	$V_{GS} = 10V$	Q_g	—	170	250	nC
Gate to Source Charge	$V_{DS} = 480V$	Q_{gs}	—	35	65	
Gate to Drain Charge	$I_D = 27A$	Q_{gd}	—	90	120	
Turn on Delay Time	$V_{GS} = 13V$	$t_{d(on)}$	—	40	75	nsec
Rise Time	$V_{DS} = 400V$	t_r	—	15	25	
Turn off Delay Time	$I_D = 27A$	$t_{d(off)}$	—	170	250	
Fall Time	$R_G = 1.8\Omega, pw = 3\mu s$	t_f	—	15	50	
Diode Forward Voltage^{4/}	$I_F = 27A, V_{GS} = 0V$	V_{SD}	—	1.1	1.3	V
Diode Reverse Recovery Time	$I_F = 10A, di/dt = 100A/\mu sec$	t_{rr}	—	130	250	nsec
	$I_F = 10A, di/dt = 100A/\mu sec$	I_{rm}	—	—	—	
	$I_F = 10A, di/dt = 100A/\mu sec$	Q_{rr}	—	—	—	
Input Capacitance	$V_{GS} = 0V$	C_{iss}	—	5050	—	pF
Output Capacitance	$V_{DS} = 100V$	C_{oss}	—	215	—	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	15	—	

CASE OUTLINE: Flat Pack (FP) - 12 Pin Package



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