Solid State Devices, Inc.
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SM720MD and SM720MM

70 mA, 35 VOLTS
8 kV ESD Rated
HIGH RELIABILITY ELECTRONIC PROTECTION ARRAY for ESD and OVERVOLTAGE PROTECTION

Designer's Data Sheet

Part Number/Ordering Information [1/]

SM720 —

Package Type
MD = 16 Pin SBDIP
MM = 20 Pin CLCC

FEATURES:

- **Military Temperature Range -55 to +125°C**
- **An Array of 14 SCR/Diode Pairs**
- **ESD Interface Capability for HBM Standards: 8 kV (ANSI / ESDA / JEDEC JS-001)**
- **IEC 61000-4-2, Direct Discharge, Single Input > 4 kV (level 2)**
  IEC 61000-4-2, Direct Discharge, Two Inputs in Parallel > 8 kV (level 4)
  IEC 61000-4-2, Air Discharge > 15 kV (level 4)
- **High Peak Surge Capability ±5 A (4 µs Single Pulse)**
- **High Reliability Hermetic Ceramic Packages**
- **Provides Over-Voltage Protection +30 V (Single Ended Voltage Range)**
- **RAD Tolerant to TID = 100 kRads** [3/]
- **Fast Switching - 2 ns Risetime**
- **No Thermal Fatigue**
- **Low Input Leakage Current - 1 nA**
- **Low Input Capacitance - 3 pF Typical**
- **Replacement for SP720MD, MM**

MAXIMUM RATINGS [2/]

RATING		SYMBOL	VALUE	UNIT
Continuous Supply Voltage		V_{SUPPLY}	35	Volts
DC Input Current		I_{IN1}	70	mAmps
Peak Input Current	(Single Pin Stress, 15V, 1 ms pulse) (Dual Pin Stress, 15V, 1 ms pulse)	I_{IN2}	2 4	Amps
Power Dissipation	SM720MD @ 93ºC SM720MM @105ºC	P_D	1	Watts
Operating Temperature Range Storage Temperature Range Maximum Junction Temperature Maximum Lead Temperature	(Soldering 10 seconds)	T_O T_{STG} T_J T_L	-55 to +125 -65 to +150 +175 +265	°C
Thermal Resistance (R$_{\theta JA}$ is measured with the component mounted on an evaluation PC board in free air)	16 Pin SBDIP 20 Pin CLCC 16 Pin SBDIP 20 Pin CLCC	$R_{\theta JC}$ $R_{\theta JA}$	18 16 80 70	°C/W

NOTES:

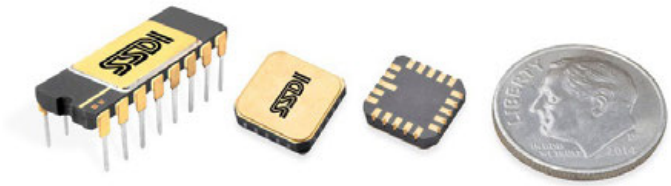
1/ For Ordering Information, Price, Operating Curves, and Availability- Contact Factory.

2/ Unless Otherwise Specified, All Electrical Characteristics @25ºC.

3/ With 18 V Bias Between V+ and V-, Electron Beam Irradiation Source.

**Dime used for size reference*

16 Pin SBDIP (MD) **20 Pin CLCC (MM)**



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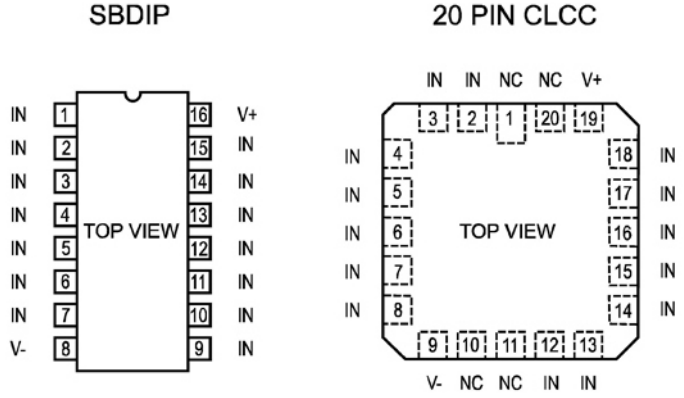
ELECTRICAL CHARACTERISTICS 2/

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Operating Voltage Range (V_{SUPPLY} = [(V+) – (V-)])	V_{SUPPLY}	0	2 to 30	**35**	Volts
Peak Forward/Reverse Voltage Drop IN to V- (with V- Reference), I_{IN} = -1 A (1 ms Peak Pulse) IN to V+ (with V+ Reference), I_{IN} = +1 A (1 ms Peak Pulse)	$V_{IN} – (V-)$ $V_{IN} – (V+)$		-2 +2		Volts
DC Forward/Reverse Voltage Drop IN to V- (with V- Reference), I_{IN} = -100 mA to V- IN to V+ (with V+ Reference), I_{IN} = +100 mA to V+	$V_{IN} – (V-)$ $V_{IN} – (V+)$	-1.5		+1.5	Volts
Input Leakage Current V- < V_{IN} < V+, V_{SUPPLY} = 30 V	I_{IN}	-15	5	+15	nA
Quiescent Supply Current V- < V_{IN} < V+, V_{SUPPLY} = 30 V	$I_{QUIESCENT}$		50	150	nA
Equivalent SCR ON Threshold			1.1		Volts
Equivalent SCR ON Resistance (V_{FWD}/I_{FWD},)			1		Ohms
Input Capacitance	C_{IN}		3		pF
Input Switching Speed	t_{ON}		2		ns

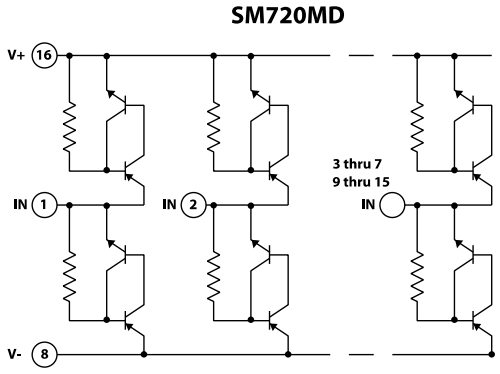
NOTES:

1/ For Ordering Information, Price, Operating Curves, and Availability- Contact Factory.
2/ Unless Otherwise Specified, All Electrical Characteristics @ 25ºC.
3/ With 18 V Bias Between V+ and V-, Electron Beam Irradiation Source.

PINOUTS:



FUNCTIONAL BLOCK DIAGRAM:



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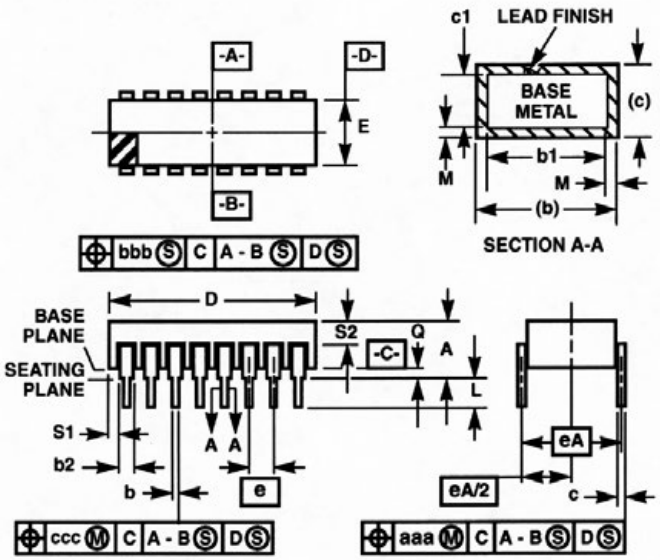
SBDIP Package Outline:

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

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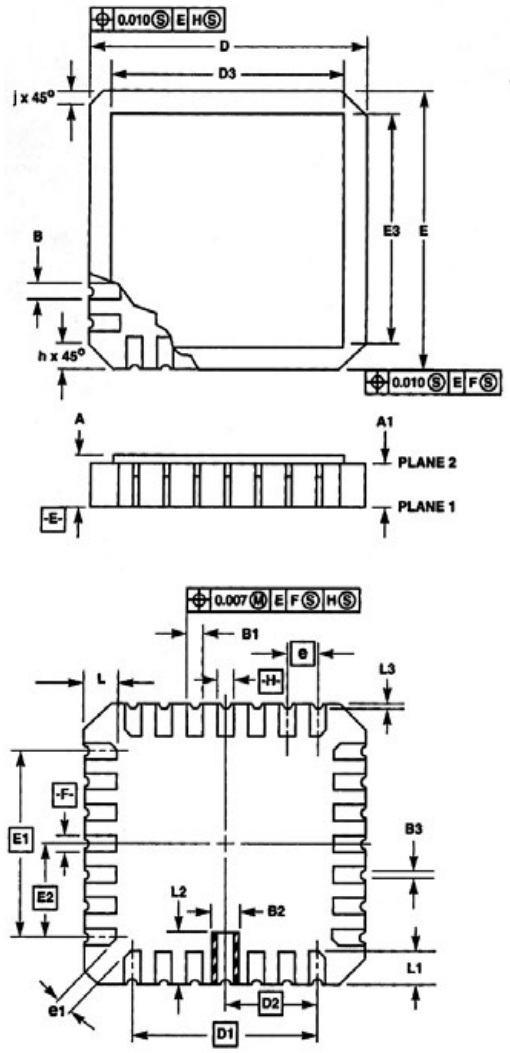
20 Pin CLCC Package Outline:

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension "A" controls the overall package thickness. The maximum "A" dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.