



Solid State Devices, Inc.

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SFF65P20S2

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF65P20

Screening ^{2/}

— = Not Screened

TX = TX Level

TXV = TXV Level

S = S Level

Package ^{3/ 4/}

S2 = SMD2

65 AMP, 200 Volts, 85 mΩ
Avalanche Rated, Enhancement Mode
P-Channel MOSFET

Features:

- PolarMOS Technology
- Lowest ON-Resistance in the Industry
- Avalanche Rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level Screening Available
- Improved ($R_{DS(ON)}$ Q_G) Figure of Merit

Maximum Ratings ^{5/}	Symbol	Value	Unit
Drain – Source Voltage	V_{DSS}	200	V
Gate – Source Voltage	V_{GS}	± 20 ± 30	V
Continuous Drain Current (T_{OP} limited) @ $T_C = 25^\circ C$	I_{D1}	65	A
Pulsed Drain Current (T_{OP} limited) @ $T_C = 125^\circ C$	I_{D2}	20	A
Single and Repetitive Avalanche Energy	E_{AS}	2500	mJ
Total Power Dissipation @ $T_C = 25^\circ C$	P_D	360	W
Operating & Storage Temperature	T_{OP} & T_{STG}	-55 to +150	$^\circ C$
Maximum Thermal Resistance (Junction to Case)	$R_{\theta JC}$	0.35 (typ. 0.3)	$^\circ C/W$

NOTES: *Pulsed per MIL-STD-750.

^{1/} For ordering information, price, and availability - contact factory.

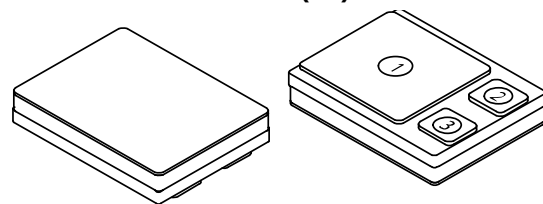
^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} For lead bending options / pinout configurations - contact factory.

^{4/} Maximum current limited by package configuration.

^{5/} Unless otherwise specified, all electrical characteristics @ $25^\circ C$.

SMD2 (S2)



NOTE: All specifications are subject to change without notification.
SSD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0100A

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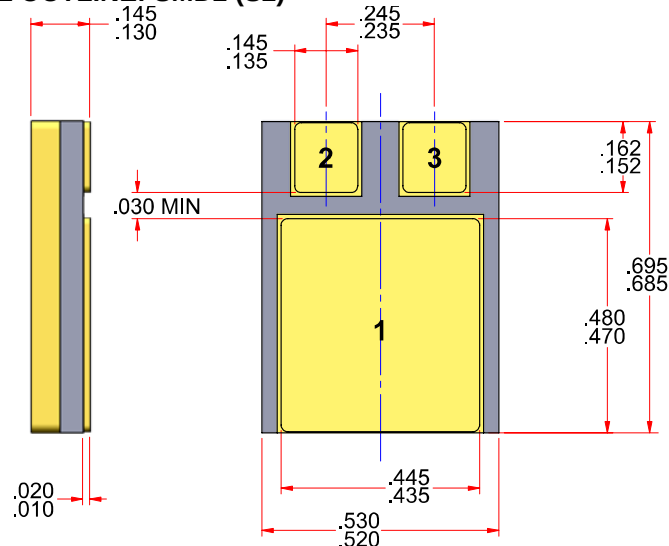
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Electrical Characteristics ^{5/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 0.25\text{ mA}$	BV_{DSS}	200	230	—	V
Drain to Source On State Resistance	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}, T_j = 25^\circ\text{C}$	$R_{DS(on)}$	—	80	85	mΩ
	$V_{GS} = 10\text{ V}, I_D = 48\text{ A}, T_j = 25^\circ\text{C}$		—	85	—	
	$V_{GS} = 10\text{ V}, I_D = 24\text{ A}, T_j = 125^\circ\text{C}$		—	150	—	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 0.25\text{ mA}, T_j = 25^\circ\text{C}$	$V_{GS(th)}$	2.0	3.3	4.0	V
	$V_{DS} = V_{GS}, I_D = 0.25\text{ mA}, T_j = 125^\circ\text{C}$		1.0	—	—	
	$V_{DS} = V_{GS}, I_D = 0.25\text{ mA}, T_j = -55^\circ\text{C}$		—	—	5.0	
Gate to Source Leakage	$V_{GS} = \pm 20\text{ V}, T_j = 25^\circ\text{C}$	I_{GSS}	—	10	±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_j = 25^\circ\text{C}$	I_{DSS}	—	0.25	25	μA
	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_j = 125^\circ\text{C}$		—	1.50	200	
Transconductance	$V_{DS} = 10\text{ V}, I_D = 24\text{ A}$	g_{fs}	18	30	—	S
Total Gate Charge	$V_{GS} = 10\text{ V}$	Q_g	—	85	—	nC
Gate to Source Charge	$V_{DS} = 100\text{ V}$	Q_{gs}	—	30	—	
Gate to Drain Charge	$I_D = 24\text{ A}$	Q_{gd}	—	33	—	
Turn on Delay Time	$V_{GS} = 10\text{ V}$	$t_{d(on)}$	—	45	—	nsec
Rise Time	$V_{DS} = 100\text{ V}$	t_r	—	60	—	
Turn off Delay Time	$I_D = 24\text{ A}$	$t_{d(off)}$	—	80	—	
Fall Time		t_f	—	45	—	
Diode Forward Voltage	$I_F = 24\text{ A}, V_{GS} = 0\text{ V}$	V_{SD}	—	2.2	3.3	V
Diode Reverse Recovery Time	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	t_{rr}	—	240	350	nsec
	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	I_{rm}	—	22	32	
	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{sec}$	Q_{rr}	—	2.6	4	
Input Capacitance	$V_{GS} = 0\text{ V}$	C_{iss}	—	5500	—	pF
Output Capacitance	$V_{DS} = 25\text{ V}$	C_{oss}	—	1020	—	
Reverse Transfer Capacitance	$f = 1\text{ MHz}$	C_{rss}	—	130	—	

CASE OUTLINE: SMD2 (S2)



PIN ASSIGNMENT (Standard)

Package	Drain	Source	Gate
SMD2	Pin 1	Pin 2	Pin 3

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