



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, CA 90638

Phone: (562) 404-4474 * Fax: (562) 404-1773

ssdi@ssdi-power.com * www.ssdi-power.com

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFL40P06 S.5



Screening ^{2/}

— = Not Screened

TX = TX Level

TXV = TXV Level

S = S Level

Package ^{3/}

S.5 = SMD.5

SFL40P06S.5

**SURFACE MOUNT
RADIATION TOLERANT
40 AMP, 60 Volts, 30 mΩ typ
Avalanche Rated P-MOSFET**

Features:

- Rugged Trench Technology
- Lowest ON-resistance in the industry: 30 mΩ typ
- Avalanche rated
- Hermetically Sealed Power Packaging
- Low Total Gate Charge, Fast Switching
- TX, TXV, S-Level screening available

Maximum Ratings	Symbol	Value	Unit
Drain - Source Voltage	V _{DSS}	-60	V
Gate - Source Voltage, continuous	V _{GS}	±15	V
Gate - Source Voltage, transient		±25	
Max. Continuous Drain Current @ T _C = 25°C (Package limited)	I _{D1} I _{D2}	40 15	A
Max. Avalanche current @ L = 5.0 mH	I _{AR}	40	A
Max. Continuous Drain Current (T _J limited)	I _{DM}	55	A
Single Pulse Avalanche Energy @ L = 5.0 mH	E _{AS}	200	mJ
Total Power Dissipation @ T _C = 25°C	P _D	63	W
Operating & Storage Temperature	T _{OP} & T _{STG}	-55 to +150	°C
Maximum Thermal Resistance (Junction to Case)	R _{θJC}	2 (typ 1.7)	°C/W

NOTES:

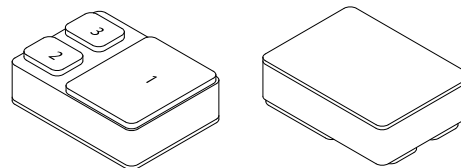
*Pulsed per MIL-STD-750.

^{1/} For ordering information, price, and availability - contact factory.

^{2/} Screening based on MIL-PRF-19500. Screening flows available on request.

^{3/} Unless otherwise specified, all electrical characteristics @ 25°C.

SMD.5 (S.5)



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0099C

DOCX



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SFL40P06S.5

Electrical Characteristics ^{3/}		Symbol	Min	Typ	Max	Unit
Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 0.25 \text{ mA}$	BV_{DSS}	-60	-65	—	V
Drain to Source On State Resistance	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(on)}$	—	27	35	mΩ
	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}, T_J = 25^\circ\text{C}$		—	30	39	
	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}, T_J = 125^\circ\text{C}$		—	45	—	
Gate Threshold Voltage	$V_{DS} = 5 \text{ V}, I_D = 250 \mu\text{A}, T_J = 25^\circ\text{C}$	$V_{GS(th)}$	-1.5	- 2.0	-3.0	V
	$V_{DS} = 5 \text{ V}, I_D = 250 \mu\text{A}, T_J = 125^\circ\text{C}$		-1.0	-1.5	—	
	$V_{DS} = 5 \text{ V}, I_D = 250 \mu\text{A}, T_J = -55^\circ\text{C}$		—	-2.3	-3.5	
Gate to Source Leakage	$V_{GS} = \pm 15 \text{ V}, T_J = 25^\circ\text{C}$	I_{GSS}	—	10	± 50	nA
	$V_{GS} = \pm 15 \text{ V}, T_J = 125^\circ\text{C}$		—	50	± 100	
Zero Gate Voltage Drain Current	$V_{DS} = -60 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	I_{DSS}	—	0.025	1	μA
	$V_{DS} = -60 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$		—	0.500	20	
Forward Transconductance	$V_{DS} = -10 \text{ V}, I_D = 15 \text{ A}, T_J = 25^\circ\text{C}$	g_{fs}	10	20	—	Mho
Total Gate Charge	$V_{GS} = -10 \text{ V}$	Q_g	—	50	—	nC
Gate to Source Charge	$V_{DS} = -32.5 \text{ V}$	Q_{gs}	—	10	—	
Gate to Drain Charge	$I_D = 15 \text{ A}$	Q_{gd}	—	15	—	
Turn on Delay Time	$V_{GS} = -10 \text{ V}$	$t_{d(on)}$	—	30	—	nsec
Rise Time	$V_{DS} = -32.5 \text{ V}$	t_r	—	35	—	
Turn off Delay Time	$I_D = 15 \text{ A}$	$t_{d(off)}$	—	110	—	
Fall Time	$R_G = 10 \Omega$	t_f	—	25	—	
Diode Forward Voltage	$I_F = 10 \text{ A}, V_{GS} = 0 \text{ V}$	V_{SD}	—	0.85	1.2	V
Diode Reverse Recovery Time	$I_F = 10 \text{ A}, di/dt = 100 \text{ A}/\mu\text{sec}$	t_{rr}	—	45	—	nsec
Peak Reverse Recovery Current		I_{RM}	—	4.0	—	A
Reverse Recovery Charge		Q_{rr}	—	90	—	nC
Input Capacitance	$V_{GS} = 0 \text{ V}$	C_{iss}	—	2300	—	pF
Output Capacitance	$V_{DS} = 25 \text{ V}$	C_{oss}	—	260	—	
Reverse Transfer Capacitance	$f = 1 \text{ MHz}$	C_{rss}	—	160	—	

PACKAGE OUTLINE:

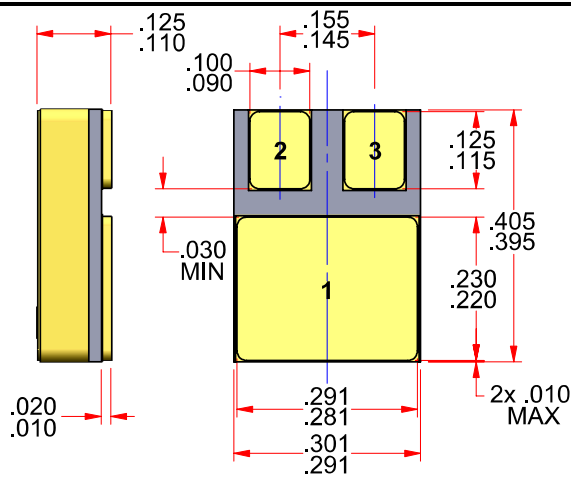
SMD.5

PINOUT:

PIN 1: DRAIN

PIN 2: SOURCE

PIN 3: GATE



Bottom View

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