



Solid State Devices, Inc.

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SGF43E70-28

43 AMP
GaN FET Normally-Off
700 VOLTS, 39 mΩ typical

Designer's Data Sheet

Part Number/Ordering Information^{1/}

SGF43E70

L Screening^{2/}

— = Not Screened
TX = TX Level
TXV = TXV Level
S = S Level

Package

-28 = LCC28

FEATURES:

- 3rd Generation Gallium Nitride Technology
- Combines GaN HEMT and Low Voltage Si MOSFET (Cascode) for Superior Performance
- Works with Common Gate Drivers
- Low RDSon
- Low Q_g Simplifies Gate Drive Circuit
- Very Fast Switching for High Frequency Applications
- Low Thermal Resistance – Internal Heat Sink
- Hermetically Sealed Surface Mount Package
- Extremely Small Footprint and Low Profile
- TX, TXV, and S-Level Screening Available^{2/}
- Available as Normally-On (without the Si Mosfet Driver)

APPLICATIONS:

- High Efficiency DC-DC / PoL Converters
- Motor Controller
- Military and Aerospace

BENEFITS:

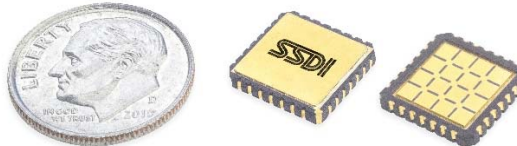
- GaN Transistor offers superior advantages over Si based MOSFET: low Q_{RR}, low gate charge, low R_{DS(ON)}, fast switching speed and low temperature coefficient
- Benefits circuit designer through higher efficiency, lower cross-over losses and On-state losses
- Eliminates the need to add free-wheeling diode

Maximum Ratings ^{3/}	Symbol	Value	Unit
Continuous Drain - Source Voltage	V _{DSS}	700	V
Transient Drain - Source Voltage In off-state, spike duty cycle D < 0.01, spike duration < 1 μs	V _{TDS}	800	V
Gate – Source Voltage	V _{GS}	±20	V
Continuous Drain Current	T _C = 25°C	I _{D1}	43 A
	T _C = 100°C	I _{D2}	23 A
Pulsed Drain Current (T _{op} / P _{width} limited)	Pulse width = 10 μs	I _{D3}	240 A
Total Power Dissipation	P _D	83	W
Operating & Storage Temperature	T _{OP} & T _{STG}	-55 to +150	°C
Thermal Resistance (Junction to Case)	R _{θJC}	1.5	°C/W

NOTES:

- 1/ For ordering information, price, operating curves, and availability-contact factory.
- 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
- 3/ Unless otherwise specified, all electrical characteristics @ 25°C.
- 4/ Pulse test, P_w = 300 μs, D.C. = 2%.

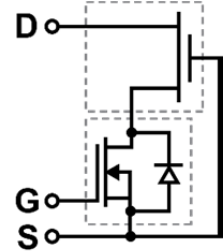
LCC28



Extremely Small Footprint: 0.458" x 0.458"

Low Profile: .095" max (dime used for size reference)

Cascode Device Structure



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0080B

DOC



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Electrical Characteristics ^{3/}	Symbol	Min	Typ	Max	Unit	
Drain to Source Breakdown Voltage	$I_D = 100 \mu A, V_{GS} = 0 V$	V_{DSS}	700	-	-	V
Gate to Source Leakage	$V_{GS} = 20V$ $V_{GS} = -20V$	I_{GSSF} I_{GSSR}	-	-	400 -400	nA
Drain to Source Leakage Current	$T_J = 25^\circ C$ $T_J = 150^\circ C$	I_{DSS}	-	3 15	25 -	μA
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1mA$	$V_{GS(th)}$	3.3	4	4.8	V
Drain to Source On State Resistance^{4/}	$T_J = 25^\circ C$ $T_J = 150^\circ C$	$R_{DS(on)}$	-	39 76	45 -	m Ω
Total Gate Charge	$V_{DS} = 400 V$	Q_g	-	24	36	nC
Gate to Source Charge	$I_D = 32 A$	Q_{gs}	-	10	-	nC
Gate to Drain Charge		Q_{gd}	-	6	-	nC
Total Output Charge	$V_{GS} = 0 V, V_{DS} = 0 V - 400 V$	Q_{OSS}	-	178	-	nC
Input Capacitance	$V_{GS} = 0 V$	C_{iss}	-	1500	-	pF
Output Capacitance	$V_{DS} = 400 V$	C_{oss}	-	190	-	pF
Reverse Transfer Capacitance	$f = 1 MHz$	C_{rss}	-	10	-	pF
Output Capacitance, Energy Related	$V_{GS} = 0 V, V_{DS} = 0 V - 400 V$	$C_{O(er)}$	-	290	-	pF
Output Capacitance, Time Related	$V_{GS} = 0 V, V_{DS} = 0 V - 400 V$	$C_{O(er)}$	-	440	-	pF
Turn-on Delay	$V_{DS} = 400 V$	$t_{D(ON)}$	-	69	-	ns
Rise Time	$V_{GS} = 12 V$	t_R	-	14	-	ns
Turn-off Delay	$I_D = 32 A$	$t_{D(OFF)}$	-	99	-	ns
Fall Time	$R_G = 30 \Omega$	t_F	-	12	-	ns
Source to Drain Forward Current^{4/}	$V_{GS} = 0 V, T_C = 100^\circ C$	I_{SD}	-	-	29.5	A
Source to Drain Forward Voltage^{4/}	$I_S = 32 A, V_{GS} = 0 V$ $I_S = 15 A, V_{GS} = 0 V$	V_{SD}	-	2.1 1.4	-	V
Source to Drain Reverse Recovery Time	$I_S = 30 A, V_{DD} = 400 V$ $di/dt=1000 A/us$	t_{RR}	-	65	-	ns
Source to Drain Reverse Recovery Charge	$I_S = 30 A, V_{DD} = 400 V$ $di/dt=1000 A/us$	Q_{RR}	-	178	-	nC

LCC28 (-28)

Top view dimensions: .040 x 45° CHAM 3 PLACES, .450±.008 SQ., .020 x 45° CHAM, PIN 1, PIN 4.

Side view dimensions: .010±.001, .095 MAX.

Bottom view dimensions: .050 REF TYP, .330 SQ., .010 TYP, .050 TYP, .025 TYP, HEAT SINK, .008 R. REF. (28 PLACES), PIN 1, PIN 4.

PIN ASSIGNMENT

Source*	12 - 18
Drain*	1 - 5, 27, 28
Gate	9
Substrate**	19, heat sink
GaN Gate**	11, 20

*All Drain / Source pins must be connected to maximize current capability and minimize $R_{DS(ON)}$
**Connect to SOURCE

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