



# Solid State Devices, Inc.

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# SGF48N20

## 48 AMP GaN POWER FET Enhancement Mode 200 VOLTS, 11 mΩ

**Designer's Data Sheet**

**Part Number/Ordering Information<sup>1/</sup>**

**SGF48N20**              

    L    **Screening<sup>2/</sup>**  
          = Not Screened  
      TX = TX Level  
      TXV = TXV Level  
      S = S Level

    L    **Package**  
          = SMG.3-1

**FEATURES:**

- 4<sup>th</sup> Generation Gallium Nitride Technology
- Exceptionally Low R<sub>DS(ON)</sub>
- Low Q<sub>G</sub> Simplifies Gate Drive Circuit
- Very Fast Switching for High-Freq. Applications
- Low Thermal Resistance Hermetically Sealed Packages - Available in Chip-Scale Package (SMG.3-1)
- TX, TXV, and S-Level Screening Available<sup>2/</sup>

**APPLICATIONS:**

- High Efficiency DC-DC/PoL Converters
- Motor Controller
- Robotics/Automation
- Military and Aerospace

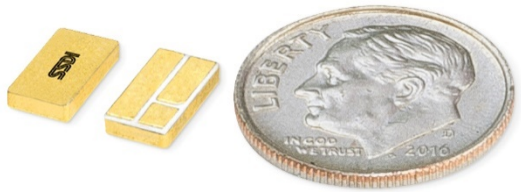
**BENEFITS:**

- GaN Transistor offers superior advantages over Si based MOSFET: Zero Q<sub>RR</sub>, low gate charge, low R<sub>DS(ON)</sub>, fast switching speed and low temperature coefficient
- Benefits circuit designer through higher efficiency, lower cross-over losses and On-state losses
- Eliminates the need to add free-wheeling diode

Maximum Ratings <sup>3/</sup>	Symbol	Value	Units
Continuous Drain - Source Voltage	V <sub>DSS</sub>	200	V
Gate – Source Voltage	V <sub>GS</sub>	+6 -4	V
Continuous Drain Current	I <sub>D1</sub>	48	A
Pulsed Drain Current (T <sub>op</sub> / P <sub>width</sub> limited)	I <sub>D2</sub>	200	A
Total Power Dissipation	P <sub>D</sub>	25	W
Operating & Storage Temperature	T <sub>OP</sub> & T <sub>STG</sub>	-55 to +150	°C
Thermal Resistance (Junction to Case)	R <sub>θJC</sub>	5	°C/W

- NOTES:**
- 1/ For ordering information, price, operating curves, and availability- contact factory.
  - 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
  - 3/ Unless otherwise specified, all electrical characteristics @ 25°C.
  - 4/ Pulse Test, P<sub>w</sub> = 300 μs, D.C. = 2%.
  - 5/ Attach device with low temperature solder such as Sn63 with peak reflow temperature of 215°C and maximum dwell time of 30 sec.

**SMG.3-1**





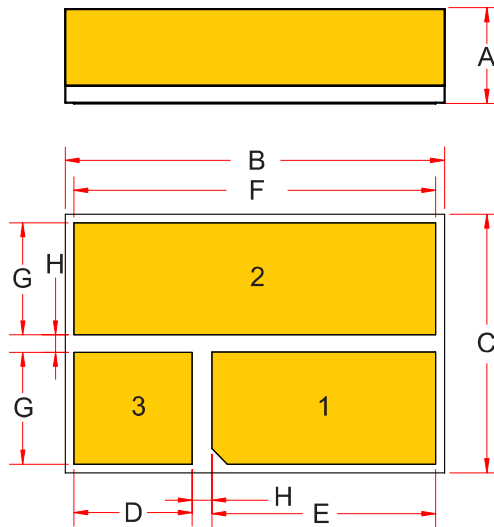
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Electrical Characteristics <sup>3/</sup>		Symbol	Min	Typ	Max	Units
<b>Drain to Source Breakdown Voltage</b>	$V_{GS} = 0\text{ V}, I_D = 0.6\text{ mA}$	$BV_{DSS}$	200	-	-	V
<b>Gate to Source Leakage</b>	$V_{GS} = +5\text{ V}$ $V_{GS} = -4\text{ V}$	$I_{GSS}$	-	1 0.1	7 0.4	mA
<b>Zero Gate Voltage Drain Current</b>	$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$	-	0.1	0.4	mA
<b>Gate Threshold Voltage</b>	$V_{DS} = V_{GS}, I_D = 7\text{ mA}$	$V_{GS(TH)}$	0.8	1.4	2.5	V
<b>Drain to Source On State Resistance<sup>4/</sup></b>	$V_{GS} = 5\text{ V}, I_D = 20\text{ A}$	$R_{DS(ON)}$	-	8	11	mΩ
<b>Source to Drain Forward Voltage<sup>4/</sup></b>	$I_F = 0.5\text{ A}, V_{GS} = 0\text{ V}$	$V_{SD}$	-	1.8	-	V
<b>Total Gate Charge</b>	$V_{GS} = 5\text{ V}, V_{DS} = 100\text{ V}, I_D = 20\text{ A}$	$Q_G$	-	12	15	nC
<b>Gate to Source Charge</b>	$V_{DS} = 100\text{ V}$ $I_D = 20\text{ A}$	$Q_{GS}$	-	3	-	nC
<b>Gate to Drain Charge</b>		$Q_{GD}$	-	1.8	-	
<b>Gate Threshold Charge</b>		$Q_{GTH}$	-	2.2	-	
<b>Input Capacitance</b>	$V_{GS} = 0\text{ V}$	$C_{ISS}$	-	950	1140	pF
<b>Output Capacitance</b>	$V_{DS} = 100\text{ V}$	$C_{OSS}$	-	450	680	
<b>Reverse Transfer Capacitance</b>	$f = 1\text{ MHz}$	$C_{RSS}$	-	2.3	-	
<b>Output Charge</b>	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}$	$Q_{OSS}$	-	75	113	nC
<b>Source to Drain Recovery Charge</b>		$Q_{RR}$	-	0	-	μC
<b>Gate Resistance</b>		$R_G$	-	0.5	-	Ω

**SMG.3-1 ( )**



DIM	MIN	MAX
A	--	.085
B	.315	.345
C	.165	.190
D	.084	.100
E	.204	.220
F	.312	.328
G	.067	.083
H	(.015)	

*Dimensions in inches*

**PIN ASSIGNMENT**

Source: 2  
 Drain: 1  
 Gate: 3  
 Substrate: \*  
 \*Substrate internally tied to Source

**AVAILABLE PART NUMBERS:**

SMG.3-1: SGF48N20

**NOTE:** All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

**DATA SHEET #: FT0073B**

**DOCX**