



PRELIMINARY

Solid State Devices, Inc.

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# SGF48N10

**48 AMP  
GaN POWER FET  
Enhancement Mode  
100 VOLTS, 6 mΩ**

## Designer's Data Sheet

### Part Number/Ordering Information<sup>1/</sup>

SGF48N10

L Screening  
\_\_\_ = Not Screened  
TX = TX Level  
TXV = TXV Level  
S = S Level

Package  
\_\_\_ = SMG.3-1

### FEATURES:

- 4<sup>th</sup> Generation Gallium Nitride Technology
- Exceptionally Low  $R_{DS(ON)}$
- Low  $Q_G$  Simplifies Gate Drive Circuit
- Very Fast Switching for High-Freq. Applications
- Low Thermal Resistance
- Hermetically Sealed, Chip-Scale Package (SMG.3-1)
- TX, TXV, and S-Level Screening Available<sup>2/</sup>

### APPLICATIONS:

- High Efficiency DC-DC / PoL Converters
- Motor Controller
- Robotics/Automation
- Military and Aerospace

### BENEFITS:

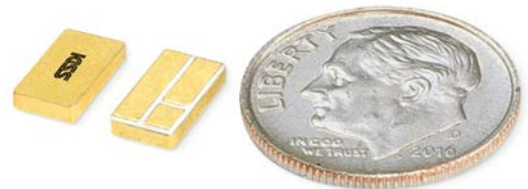
- GaN Transistor offers superior advantages over Si based MOSFET: zero  $Q_{RR}$ , low gate charge, low  $R_{DS(ON)}$ , fast switching speed and low temperature coefficient
- Benefits circuit designer through higher efficiency, lower cross-over losses and On-state losses
- Eliminates the need to add free-wheeling diode

Maximum Ratings <sup>3/</sup>	Symbol	Value	Units
Continuous Drain - Source Voltage	$V_{DSS}$	100	V
Gate - Source Voltage	$V_{GS}$	+6 -4	V
Continuous Drain Current	$I_{D1}$	48	A
Pulsed Drain Current $T_{op} / P_{width}$ limited	$I_{D2}$	340	A
Total Power Dissipation	$P_D$	25	W
Operating & Storage Temperature	$T_{OP} \& T_{STG}$	-55 to +150	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	5	°C/W

### NOTES:

- 1/ For ordering information, price, operating curves, and availability- contact factory.
- 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
- 3/ Unless otherwise specified, all electrical characteristics @ 25°C.
- 4/ Pulse Test,  $P_w = 300 \mu s$ , D.C. = 2%.
- 5/ Attach device with low temperature solder such as Sn63 with peak reflow temperature of 215°C and maximum dwell time of 30 sec.

SMG.3-1 (\_\_\_)



NOTE: All specifications are subject to change without notification. SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0071A

DOC



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Electrical Characteristics <sup>3/</sup>	Symbol	Min	Typ	Max	Units
<b>Drain to Source Breakdown Voltage</b> $V_{GS} = 0\text{ V}, I_D = 0.8\text{ mA}$	$BV_{DSS}$	100	-	-	V
<b>Gate to Source Leakage</b> $V_{GS} = +5\text{ V}$ $V_{GS} = -4\text{ V}$	$I_{GSS}$	-	1 0.1	9 0.6	mA
<b>Zero Gate Voltage Drain Current</b> $V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$	$I_{DSS}$	-	0.1	0.6	mA
<b>Gate Threshold Voltage</b> $V_{DS} = V_{GS}, I_D = 11\text{ mA}, T_J = 25^\circ\text{C}$	$V_{GS(th)}$	0.8	1.4	2.5	V
<b>Drain to Source On State Resistance<sup>4/</sup></b> $V_{GS} = 5\text{ V}, I_D = 30\text{ A}, T_J = 25^\circ\text{C}$	$R_{DS(on)}$	-	5.5	6	m $\Omega$
<b>Source to Drain Forward Voltage<sup>4/</sup></b> $I_F = 0.5\text{ A}, V_{GS} = 0\text{ V}$	$V_{SD}$	-	1.8	-	V
<b>Total Gate Charge</b> $V_{GS} = 5\text{ V}, V_{DS} = 50\text{ V}, I_D = 30\text{ A}$	$Q_G$	-	12	15	nC
<b>Gate to Source Charge</b> <b>Gate to Drain Charge</b> <b>Gate Threshold Charge</b> $V_{DS} = 50\text{ V}$ $I_D = 30\text{ A}$	$Q_{GS}$ $Q_{GD}$ $Q_{GTH}$	-	3.1 2 2.3	10 4 4.6	nC
<b>Input Capacitance</b> <b>Output Capacitance</b> <b>Reverse Transfer Capacitance</b> $V_{GS} = 0\text{ V}$ $V_{DS} = 50\text{ V}$ $f = 1\text{ MHz}$	$C_{ISS}$ $C_{OSS}$ $C_{RSS}$	-	1270 800 14	1530 1200 -	pF
<b>Output Charge</b> $V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$	$Q_{OSS}$	-	66	100	nC
<b>Source to Drain Recovery Charge</b>	$Q_{RR}$	-	0	-	$\mu\text{C}$
<b>Gate Resistance</b>	$R_G$	-	0.4	-	$\Omega$

**Case Outline: SMG.3-1 ( )**

**Available Part Numbers:**  
SMG.3-1: SGF48N10

**Pin Assignment**  
Source: 2  
Drain: 1  
Gate: 3  
Substrate: internally tied to Source

Dimensions (in inches)		
DIM	MIN	MAX
A	--	.085
B	.315	.345
C	.165	.190
D	.084	.100
E	.204	.220
F	.312	.328
G	.067	.083
H	(.015)	

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