



Solid State Devices, Inc.

14830 Valley View Blvd * La Mirada, CA 90638

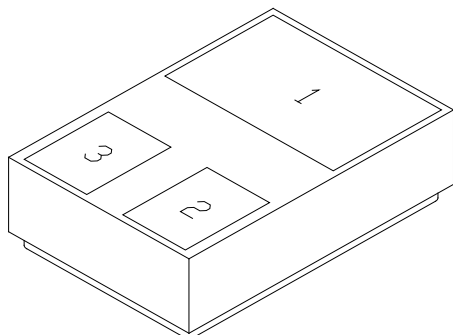
Phone: (562) 404-7855 * Fax: (562) 404-1773

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SFF110S.22

SFF110S.22C

DESIGNER'S DATA SHEET



SMD.22

3.5 A /100 Volts / 0.6 Ω

N-Channel MOSFET Transistor

Features:

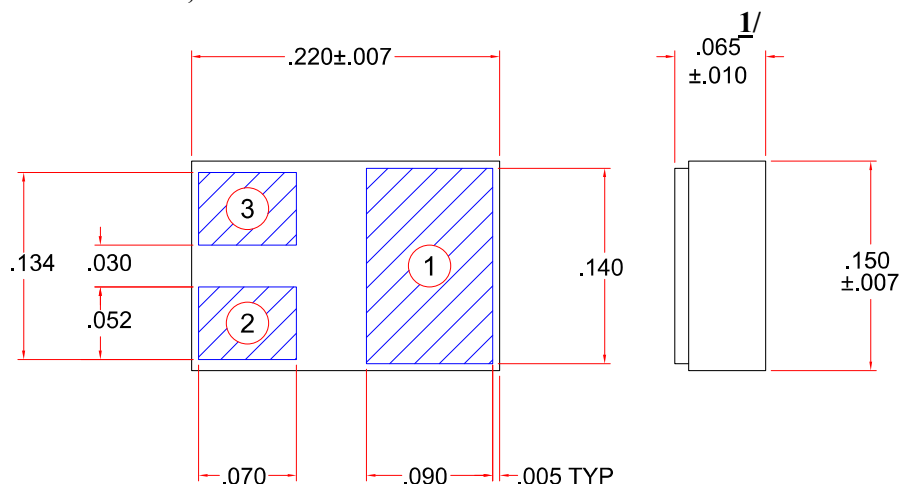
- Available with ceramic lid as SFF100S.22C
- Small Footprint Hermetic Surface Mount Device with Excellent Thermal Properties
- Replacement/Enhancement for 2N6782
- TX, TXV, S-Level Screening Available
- Very Fast Switching Characteristics

Maximum Ratings	Symbol	Value	Units
Drain – Source Voltage	V_{DS}	100	Volts
Drain – Gate Voltage	V_{DG}	100	Volts
Gate – Source Voltage	V_{GS}	+/-20	Volts
Continuous Drain Current	I_{D1} I_{D2}	3.5 2.25	Amps
Power Dissipation @ $T_C = 25^\circ C$	P_D	16.5	W
Power Dissipation @ $T_A = 25^\circ C$		0.8	
Avalanche Energy, nonrepetitive	E_{as}	7	mJ
Operating & Storage Temperature	Top & Tstg	-55 to +150	$^\circ C$
Maximum Thermal Resistance	$R_{\theta JC}$ $R_{\theta JA}$	7.5 (typ 5)	$^\circ C/W$
Junction to Case and to Ambient		156.5	

Note1: Derated 60.6 mW/ $^\circ C$ above $T_C = 25^\circ C$

Note2: Derated 6.4 mW/ $^\circ C$ above $T_A = 25^\circ C$

PAD 1= DRAIN; PAD 2= SOURCE; PAD 3= GATE



1/ **Note:** For SMD.22C (Ceramic Lid) Package Height = .070±.010"

NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

DATA SHEET #: FT0015B

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Electrical Characteristics ^{4/}		Symbol	Min	Typ	Max	Units
Drain – Source Breakdown Voltage	$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	BV_{DSS}	100	110	—	Volts
Gate – Source Threshold Voltage	$V_{DS} = 4 \text{ V}; I_D = 0.25 \text{ mA}$ $V_{DS} = 4 \text{ V}; I_D = 0.25 \text{ mA}; T_A = 125^\circ\text{C}$ $V_{DS} = 5 \text{ V}; I_D = 0.25 \text{ mA}; T_A = -55^\circ\text{C}$	$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	2.0 1.5 —	3.0 2.5 3.4	4.0 — 4.5	Volts
Gate Leakage Current	$V_{GS} = \pm 20 \text{ V}$ $V_{GS} = \pm 20 \text{ V}, T_A = 125^\circ\text{C}$	I_{GSS1} I_{GSS2}	— —	25 50	100 200	nA
Drain Leakage Current	$V_{GS} = 0 \text{ V}; V_{DS} = 80 \text{ V}$ $V_{GS} = 0 \text{ V}; V_{DS} = 80 \text{ V}, T_A = 125^\circ\text{C}$	I_{DSS1} I_{DSS2}	— —	0.05 0.15	25 100	μA
Static Drain – Source On-State Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.25 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 3.50 \text{ A}$	$R_{DS(on)1}$ $R_{DS(on)2}$	— —	0.38 0.40	0.50 0.55	Ohm
	$V_{GS} = 10 \text{ V}, I_D = 2.25 \text{ A}, T_A = 125^\circ\text{C}$	$R_{DS(on)3}$	—	0.67	1.0	
Forward Voltage of the Source – Drain Diode	$I_D = 3.5 \text{ A}$	V_{SD}	—	1.0	1.2	Volts
Switching Time Test: Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$I_D = 3.5 \text{ A}, V_{GS} = 10 \text{ V},$ $R_G = 7.5 \text{ ohm}, V_{DD} = 50 \text{ V}$	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	— — — —	15 10 20 10	25 15 35 15	ns
Gate Charge Test: On-State Gate Charge Gate – Source Charge Gate – Drain Charge	$V_{GS} = 10 \text{ V}, V_{DS} = 50 \text{ V}$	$Q_{g(on)}$ Q_{gs} Q_{gd}	— — —	6.5 2 2.15	7.5 2.5 3.0	nC
Reverse Recovery Time Reverse Recovery Current	$V_{DD} = 50 \text{ V}, I_F = 3.5 \text{ A},$ $dI/dt = 100 \text{ A}/\mu\text{s}$	t_{rr} I_{rm}	— —	85 6.6	180 —	Ns A
Capacitance Test: Input Capacitance Output Capacitance Reverse Transfer Cap.	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	C_{iss} C_{oss} C_{rss}	— — —	180 85 15	— — —	pF

NOTES:

* Pulse Test: Pulse Width = 300 μsec , Duty Cycle = 2%

^{1/} For Ordering Information, Price, Availability Contact Factory.

^{2/} Screening per MIL-PRF-19500

^{3/} For Package Outlines Contact Factory.

^{4/} Unless Otherwise Specified, All Electrical Characteristics @25°C.

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